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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,591	10/20/2003	Yoshihiro Takemae	108397-00109	2535

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ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
SUITE 400
1050 CONNECTICUT AVENUE, N.W.
WASHINGTON, DC 20036-5339

EXAMINER	
KIM, DANIEL Y	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,591	TAKEMAE, YOSHIHIRO	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *1-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-26* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on October 20, 2003 was filed after the mailing date of the parent application on January 29, 2002. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10057989, filed on January 29, 2002.

Claim Objections

3. Claim 20 is objected to because of the following informalities:
In claim 20, line 2, it appears that after "second interface", "unit" should be changed to "portion". There was no previous mention of a "unit" in the recited claims. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 16-17 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda (US PGPub No. 20010054135) and Akamatsu et al (US Patent No. 5,983,331).

For claim 16, Matsuda discloses a common memory controller capable of controlling different types of memory chips (a memory controller having general versatility and enhanced extensibility to allow different types of memory devices to be supported is disclosed, 20010054135, abstract), comprising:

a first interface portion for receiving a control output signal to access said memory chip from a controller, and outputting a control input signal to the controller (an interface device connecting a processor and a memory device through a bus, including a memory controller for controlling data communication with the memory device, par. 0015);

a conversion control portion for converting said control output signal into a memory input signal in response to a specification of a memory chip to which the memory controller is connected, and converting a memory output signal output from the memory chip into the control input signal receivable to said controller (a level adjuster for adjusting a voltage level of dara to be transferred between the memory device and the data bus depending on a type of the memory device, par. 0011; the selector determines access mode from data and address data on an address/data bus to output access mode control data, par. 0032); and

a second interface portion for outputting the memory input signal and receiving the memory output signal (par. 0015).

Despite these teachings, Matsuda fails to disclose a plurality of terminals coupled to the second interface portion, and capable of connecting at least one of the different types of memory chips.

Akamatsu, however, discloses a semiconductor system with a plurality of chips, wherein a terminal section is made up of terminal blocks and each terminal block is employed for connection with a respective subsidiary chip. An interface circuit has mode output circuits and mode input circuits corresponding to subsidiary chips (col. 9, lines 33-38).

Akamatsu and Matsuda are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a plurality of terminals to be coupled to an interface for controlling different types of memory chips, because this allows for connection with a plurality of different subsidiary chips (col. 9, lines 35-38), as taught by Akamatsu.

For claim 17, the combined teachings of Matsuda and Akamatsu disclose the invention as per the rejection of claim 16 above. Matsuda further discloses the different types of memory chips include a synchronous DRAM or a synchronous SRAM (in the case where the memory device is a synchronous RAM, the mode controller selects the clock signal to supply it as the timing control signal to the first buffer. In the case where the memory is a double data rate synchronous RAM, the mode controller selects the

data strobe signal to supply it as the timing control signal to the first and second buffers, par. 0013).

For claim 20, the combined teachings of Matsuda and Akamatsu disclose the invention as per the rejection of claim 16 above. Matsuda further discloses the second interface unit controls an output timing of the memory input signal in response to the specification of memory chip (a mode controller for controlling the timing control signal to meet timing requirement of the memory device depending on a mode selection signal inputted from outside, par. 0010).

For claim 21, the combined teachings of Matsuda and Akamatsu disclose the invention as per the rejection of claim 16 above. Matsuda further discloses the memory input signal includes an address, a command, and data (the CPU supplies data and address data to the selector, the refresh circuit and the address/data switch through the address/data bus. The address/data switch divides data and address data on the address/data bus respectively to the data buffer and the address signal generator depending on the control signal from the control signal generator, par. 0033).

6. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda (US PGPub No. 20010054135), Akamatsu et al (US Patent No. 5,983,331) and Smith (US Patent No. 6,085,317).

For claim 18, the combined teachings of Matsuda and Akamatsu disclose the invention as per the rejection of claim 16 above. Matsuda and Akamatsu fail to disclose,

however, a memory unit for storing the specification of the memory chip, and wherein the memory unit is programmable.

Smith, however, discloses a configuration data set suitable for reconfiguring the programmable logic units may be stored in a memory unit (col. 3, lines 39-41).

Smith, Matsuda and Akamatsu are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a programmable memory unit for storing the specification of the memory chip because this would allow the entire system to be dynamically changed in response to a system condition or to by dynamically upgraded (col. 3, lines 36-38), as taught by Smith.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda (US PGPub No. 20010054135), Akamatsu et al (US Patent No. 5,983,331) and Prouty et al (US Patent No. 6,470,433).

For claim 19, the combined teachings of Matsuda and Akamatsu disclose the invention as per the rejection of claim 16 above. Matsuda and Akamatsu fail to disclose, however, the specification of memory chip includes a memory type, a command sequence, an address sequence or latency information.

Prouty, however, discloses a signaler translates command indications coming from command processor into the timing and assertion levels required as dictated by the chip specification (col. 8, lines 40-44).

Prouty, Matsuda and Akamatsu are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include command indications on a specification of memory chip because this allows the chip to be driven by a signaler accordingly, so that indications such as activate, precharge, etc. may be translated (col. 8, lines 38-49), as taught by Prouty.

8. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda (US PGPub No. 20010054135), Akamatsu et al (US Patent No. 5,983,331) and Takeda (US PGPub No. 20010011311).

For claim 22, the combined teachings of Matsuda and Akamatsu disclose the invention as per the rejection of claims 16 and 21 above. Matsuda and Akamatsu fail to disclose, however, the memory input signal further includes a chip select signal.

Takeda, however, discloses a function informs the memories and the input/output circuits of which memory or input/output circuit is selected by the CPU and initiates a data transfer; this function is regarded as "chip enable control" (par. 0004).

Takeda, Matsuda and Akamatsu are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a chip select signal with the memory input signal because this allows logic operations between the signals indicating kinds of addressing and access to be carried accordingly (par. 0004), as taught by Takeda.

For claim 23, the combined teachings of Matsuda and Akamatsu disclose the invention as per the rejection of claims 16 and 21 above. Matsuda and Akamatsu fail to disclose, however, the memory input signal further includes a direct memory access control signal.

Takeda, however, discloses a circuit such as a direct memory access controller (par. 0079).

Takeda, Matsuda and Akamatsu are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a direct memory access control signal with the memory input signal because this allows data transfer control in a fast manner (par. 0079), as taught by Takeda.

9. Claims 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda (US PGPub No. 20010054135), Akamatsu et al (US Patent No. 5,983,331) and Suzuki (US PGPub No. 20030070049).

For claim 24, the combined teachings of Matsuda and Akamatsu disclose the invention as per the rejection of claim 16 above. Matsuda and Akamatsu fail to disclose, however, the number of the plurality of terminals is larger than that of the terminals of each of the memory chips to which the memory controller is connected.

Suzuki, however, discloses an LSI with a plurality of circuit modules accessing data to a memory device on one LSI. These LSI share one or more memory devices by all the circuit modules performing a memory access on the LSI to limit the number of

terminals of the LSI. Therefore, one memory control circuit is mounted on the LSI and the circuit modules performing a memory access on the LSI perform a memory access via the memory control circuit (par. 0006).

Suzuki, Matsuda and Akamatsu are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to reduce the plurality of terminals on these memory chips because this would reduce the parts cost of the entire system using the LSI (par. 0006), as taught by Suzuki.

For claim 26, the combined teachings of Matsuda and Akamatsu disclose the invention as per the rejection of claim 16 above. Matsuda and Akamatsu fail to disclose, however, a system LSI chip to be coupled to the invention as described therein.

Suzuki, however, discloses one memory control circuit is mounted on an LSI chip and the circuit modules performing a memory access on the LSI perform a memory access via the memory control circuit (par. 0006).

Suzuki, Matsuda and Akamatsu are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include an LSI chip to be coupled to the invention because this allows for aid in quick completion of memory accesses having a time limit in the case of contention of memory accesses (abstract), as taught by Suzuki.

10. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda (US PGPub No. 20010054135), Akamatsu et al (US Patent No. 5,983,331) and Funaba et al (US PGPub No. 20020159284).

For claim 25, the combined teachings of Matsuda and Akamatsu disclose the invention as per the rejection of claim 16 above. Matsuda and Akamatsu fail to disclose, however, the plurality of terminals include control terminals, address terminals, data terminals, and a clock terminal.

Funaba, however, disclose the memory module has module data terminal pairs, a module command/address terminal pair, and a module clock terminal pair (par. 0098).

Funaba, Matsuda and Akamatsu are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include these types of terminals because this allows a controller to be capable of controlling memory operations by providing a means for connecting the memory system to the controller to enable such (abstract), as taught by Funaba.

Citation of Pertinent Prior Art

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ogawa (US Patent No. 5,804,987) discloses an LSI chip with a latch controller for sending program signal to be generated when program data is input to the chip and

transferring program data to latch circuits in a memory system in synchronism with a clock signal.

Mergard et al (US Patent No. 6,415,348) discloses a microcontroller with a flexible architecture including memory controllers to control timing and addressing, and a chip select unit.

Contact Information

12. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

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PIERRE VITAL
PRIMARY EXAMINER